REMARKS/ARGUMENTS

The present Amendment is in response to the Office Action having a mailing date of March 18, 2004. Claims 1 and 4-20 remain pending in the present application.

Applicant has presented arguments below that Applicant believes should render the claims allowable. In the event, however, that the Examiner is not persuaded by Applicant's arguments, Applicant respectfully requests that the Examiner enter the amendments and remarks to clarify issues upon appeal.

Drawings

The Examiner states:

Figures 1-3 are objected to under section 608.02(1) in the M.P.E.P. Portions of the figures are not consistent with the requirements as set forth in the aforementioned section, specifically with regards to "Every line, number, and letter must be...sufficiently dense and dark, and uniformly thick and well defined," Correction is required.

Applicant will provide drawing sheets for Figs. 1, 2, and 3 consistent with the MPEP when the application is allowed.

For the reasons set forth more fully below, Applicant respectfully submits that the present claims are allowable. Consequently, reconsideration allowance and passage to issue of the present application are respectfully requested.

Cited Art Rejections

The Examiner rejected: Claims 1, 15, 18 under 35 U.S.C. 102(b) as being anticipated by Ohhata et al., U.S. 5,402,377; Claims 4, 6-7, 16-17, 19 under 35 U.S.C. 103(a) as being

unpatentable over Ohhata et al., U.S. 5,402,377, in view of Bhavsar et al., U.S. 6,408,401; Claims 5, 8-12 under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al. U.S. 5,402,377, in view of Douceur, U.S. 5,838,893; Claims 13-14 under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al. U.S. 5,402,377, in view of Douceur, U.S. 5,838,893, and in further view of Bhavsar et al., U.S. 6,408,401; and Claim 20 under 35 U.S.C. 103(a) as being unpatentable over Ohhata et al., U.S. 5,402,377, in view of Bhavsar et al., U.S. 6,408,401, and Torrance et al. "A 33 GB/s 13.4 Mb Integrated Graphics Accelerator and Frame Buffer," IEEE International Solid-State Circuits Conference 1998.

Applicant respectfully disagrees with the rejections.

In the present invention, a cache is provided for a memory unit of an embedded memory device. Attempts to access a failed bit memory location in the memory unit are determined. When a failed memory bit location is being accessed, substitution of a memory location in the cache for the failed bit memory location occurs via a look-up table, where the look-up table is also provided in the cache.

Independent Claims

1. A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

providing a cache for a memory unit;

determining when an access is made to a failed bit memory location in the memory unit, wherein determining when an access is made further comprises identifying each failed bit location in the memory unit and storing each failed bit location in the cache, wherein storing further comprises storing each failed bit location in a look-up table; and

substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed.

8. A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

performing a memory pre-scan operation on an embedded memory device to identify each failed bit location in the embedded memory device;
storing each failed bit location in a look-up table; and
swapping a memory location within a cache for a failed bit location.

15. An embedded memory device with increased yield of usable memory locations, the embedded memory device comprising:
a memory unit;
a cache coupled to the memory unit; and
a memory control unit coupled to the memory unit and the cache, the memory control unit determining when an access is made to a failed bit memory location in the memory unit, and substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed, wherein determining when an access is made further comprises identifying each failed bit location in the memory unit and storing each failed bit location in the cache, wherein storing further comprises storing each failed bit location in a look-up table.

With the present invention, an efficient approach to increasing embedded memory device yield is provided. The provision of a cache to substitute for failed memory locations in a memory portion of the embedded memory device allows utilization of memory space substantially equivalent to the intended size of the memory portion. In this manner, the number of usable memory bit locations or yield of the memory portion is increased over prior art approaches of memory re-mapping. Further, the ability to maintain utilization of an embedded memory device with failed bit locations increases production yield, since fewer devices would need to be discarded.

ARGUMENTS

In the rejection of independent claims 1 and 15, the Examiner contends that:

Ohhata teaches to identifying a failed bit location in the memory device, and storing a failed bit location in the cache (Fig. 2; Col. 2: 60-67). The cache allows for cell defect signals to be produced based on the aforementioned

stored defect information, therefore, providing all the functionality of a look-up table, that is, storing and retrieving data related to the identification of a failed bit location and identification of the address of said failed location (Col. 15: 42-52).

In the rejection of independent claim 8, the Examiner contends that:

Ohhata does not teach of a method including a pre-scan operation on the memory array for the purpose of identifying a failed memory cell location. Douceur teaches that it is known to make a determination of faulty memory cell locations upon device startup (Col. 1:47-56). It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the testing methodology set forth by Douceur in the method provided by Ohhata because testing at startup allows for an early determination to be made on the error status of the memory cell location (Douceur, Col. 1: 55-56).

As per claim 8:
Shown above is a combination of Douceur and Ohhata that allows for a pre-scan operation to be performed whereby a memory location is swapped into a cache location. Moreover, it has been shown above that Ohhata teaches to the storage of each failed bit location in a look-up table (Col. 2: 60-67).

With regard to the cited art of Ohhata, Applicant fails to see any teaching or suggestion of a secondary memory array that provides a cache for a memory unit. Rather, Ohhata merely shows two memory cell arrays, a primary and a secondary, in the cited Figure 2 and offers no teaching or suggestion that the secondary array is a cache. Thus, Ohhata fails to teach, show, or suggest the swapping of a defective memory cell location of a memory unit with a memory location in a cache, as recited in Applicant's independent claims 1, 8, and 15.

Further, the Examiner argues that the secondary 'cache' memory array acts as a look-up table, storing failed bit locations. Applicant respectfully disagrees. There is nothing to teach or suggest that address data of a defective memory cell being stored in Ohhata is done in a look-up table format nor that failed bit locations are stored in the secondary memory array. Rather, it is the non-volatile memory cell in Ohhata that is taught as storing addresses of defective cells of the

primary array without teaching or suggesting the use of a look-up table in the non-volatile memory (Col 2: 60-67). Therefore, even if the secondary memory cell were somehow construed as a 'cache', there is nothing to teach or suggest that the secondary 'cache' memory cell stores defective cell addresses. Furthermore, there can be nothing to teach or suggest that the 'cache' stores a look-up table of defective cell addresses. Accordingly, Applicant respectfully submits that the cited art of Ohhata fails to teach, show, or suggest the recited invention, as contended by the Examiner. Further, even the inclusion of one or more of the other cited art references with Ohhata fails to overcome these deficiencies of Ohhata.

For the above-mentioned reasons the independent claims are allowable over the cited references. Moreover dependent claims 4-7, 9-14 and 16- 20 are allowable since they depend from an allowable base claim.

Applicant respectfully requests reconsideration and allowance of claims 1 and 4-20.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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Date

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